REMARKS

Applicant has reviewed and considered the Office Action mailed on December 20, 2006, and the references cited therewith.

Claims 1 and 19 are amended. Claims 1-31 are still pending in this application.

35 USC § 102 Rejection of the Claims

Claims 1, 4, 13, 19, 27-31 were rejected under 35 USC § 102(e) as being anticipated by *Sugar et al.* (U.S. Patent 6,728,517).

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Emphasis added.

Please note that no part of the present response is to be deemed an admission that Sugar et al., a 35 USC § 102(e) reference, is valid prior art in the present application. As such, the Applicants reserve the right to swear behind this reference at a later date.

Claim 1 is an independent claim directed to a module that comprises a substrate and first, second, and third microelectronic dice that are mounted on the substrate. The first and second microelectronic dice each include a receiver front end for a corresponding antenna. The third microelectronic die includes analog baseband circuitry to process baseband output signals of the first and second receiver front ends. The module also includes a first interconnect coupled between an output of the first microelectronic die and a first input of the third microelectronic die and a second interconnect coupled between an output of the second microelectronic die and a second input of the third microelectronic die.

Sugar et al. does not disclose first, second, and third microelectronic dice mounted on a substrate, where the first and second microelectronic dice each include a receiver front end for a corresponding antenna and the third microelectronic die includes analog baseband circuitry to process baseband output signals of the first and second receiver front ends. In addition, Sugar et al. discloses neither "a first interconnect coupled between an output of the first microelectronic

die and a first input of the third microelectronic die" nor "a second interconnect coupled between an output of the second microelectronic die and a second input of the third microelectronic die." The Examiner takes the position that Sugar et al. discloses first, second, and third microelectronic dice mounted on a substrate. The Applicants respectfully disagree. As stated in the Abstract of Sugar et al., as identified by the Examiner, "The radio transceiver provides, on a single semiconductor integrated circuit, a receiver circuit or path ...". Similar language is found in column 1, lines 47-48 of Sugar et al., in column 1, lines 58-60 of Sugar et al., as well as in multiple other locations. Thus, all of the elements in Sugar et al. identified by the Examiner in connection with claim 1 are located within a single integrated circuit, and not within multiple dice.

Sugar et al. even teaches away from using multiple different microelectronic dice. For example, at column 1, line 66 to column 2, line 10, it states, "In such an application, it is very important that each of the receive processing paths and each of the transmit processing paths be matched in terms of amplitude and phase response. Because the multiple receive and transmit paths are integrated into a single semiconductor die, the processing paths will inherently be better phase and amplitude matched, and any effects resulting from semiconductor integration will track among the processing paths. Moreover, any operational changes due to temperature variations will also better track among the processing paths because they are integrated into the same semiconductor integrated circuit." (Emphasis added.) Claim 1 of the present application has been amended herein to more clearly define the first, second, and third microelectronic dice as being different from one another.

Based on the foregoing, it is submitted that claim 1 of the present application is not anticipated by Sugar et al. Reconsideration and allowance of claim 1 is therefore respectfully requested. Independent claim 19 is allowable for at least the same reasons.

Claim 13 is an independent claim that is directed to a multi-antenna receiver system that comprises: (a) a first low noise amplifier (LNA) having a differential input to receive a signal from a first antenna; (b) a second LNA having a single-ended input to receive a signal from a second antenna; (c) a first mixer to perform a frequency conversion on an amplified output signal of said first LNA; (d) a second mixer to perform a frequency conversion on an amplified output

signal of said second LNA; and (e) a voltage controlled oscillator (VCO) to provide a local oscillator signal to said first and second mixers.

The Examiner has identified receiver circuit 140 of Fig. 2 of Sugar et al., and associated text, as disclosing an LNA having a differential input and receiver circuit 170 of Fig. 2 of Sugar et al., and associated text, as disclosing an LNA having a single ended input. However, nowhere in Fig. 2 or in the identified text does it disclose, either expressly or inherently, that an LNA within receiver circuit 140 has a differential input and an LNA within receiver circuit 170 has a single ended input. Therefore, Sugar et al. does not disclose all of the limitations of claim 13. If the Examiner maintains this rejection, it is respectfully requested that he identify, with specificity, where Sugar et al. is disclosing these limitations or why these limitations are believed to be inherent.

Based on the foregoing, it is submitted that claim 13 of the present application is not anticipated by Sugar et al. Reconsideration and allowance of claim 13 is therefore respectfully requested.

Claim 27 is an independent claim directed to a method comprising: (a) amplifying a first signal received by a first antenna using a differential low noise amplifier (LNA) to generate an amplified first signal; (b) amplifying a second signal received by a second antenna using a single ended LNA to generate an amplified second signal; and (c) processing said amplified first signal and said amplified second signal to generate a single receiver output signal.

In a similar fashion to the argument set out above in connection with claim 13, Sugar et al. does not disclose, either expressly or inherently, amplifying a first signal using a differential LNA to generate an amplified first signal; amplifying a second signal using a single ended LNA to generate an amplified second signal; and processing the amplified first and second signals to generate a single receiver output signal. As before, if the Examiner maintains this rejection, it is respectfully requested that he identify, with specificity, where Sugar et al. is disclosing these limitations or why these limitations are believed to be inherent.

Based on the foregoing, it is submitted that claim 27 of the present application is not anticipated by Sugar et al. Reconsideration and allowance of claim 27 is therefore respectfully requested.

Claim 4 and claims 28-31 are dependent claims that depend, either directly or indirectly, from independent claims 1 and 27, respectively. Consequently, these claims are allowable for at least the same reasons as their respective base claims. These claims also provide further bases for patentability. For example, claim 4 further defines at least one of the first interconnect and the second interconnect of claim 1 as including a microstrip transmission line formed on the substrate. As described previously, the "first interconnect" of claim 1 is coupled between an output of the first microelectronic die and a first input of the third microelectronic die and the "second interconnect" of claim 1 is coupled between an output of the second microelectronic die and a second input of the third microelectronic die. Sugar et al. does not disclose, either expressly or inherently, the use of a microstrip line to connect an output of a microelectronic die (first or second) having a receiver front end to another microelectronic die (third) that includes analog baseband circuitry. The Examiner takes the position that Sugar et al. discloses the microstrip interconnect of claim 4 in column 12, line 66 to column 13, line 2. The Applicants respectfully disagree. This passage is referring to a quarter wave transformer 515 (see Fig. 8 of Sugar et al.) that is used to generate an open circuit at an input thereto when a transmit/receive switch 112 is in the transmit position. This passage does not disclose a microstrip interconnect connecting two microelectronic dice, as defined in the claims.

35 USC § 103 Rejection of the Claims

Claims 2, 3, 5-12, 14-18, 20-26 were rejected under 35 USC § 103(a) as being unpatentable over *Sugar et al.* (US Patent 6,728,517).

Claims 2-3 and 5-12, claims 14-18, and claims 20-26 are dependent claims that depend either directly or indirectly from independent claims 1, 13, and 19, respectively. Consequently, these claims are allowable for at least the same reasons as their corresponding base claims. These claims also provide further bases for patentability. For example, claim 10 adds to the module of claim 1 a "third interconnect coupled between said first microelectronic die and said second microelectronic die." As described previously, Sugar et al. does not disclose a "first microelectronic die" and a different "second microelectronic die" as those elements are defined in claim 1. Therefore, Sugar et al. does not disclose an interconnect between such dice. Claim 11 further defines (a) the "first receiver front end" of claim 10 as including "a first low noise

amplifier (LNA) to amplify a signal from a first antenna and a first mixer to frequency convert an output signal of said first LNA," (b) the "said second receiver front end" of claim 10 as including "a second LNA to amplify a signal from a second antenna and a second mixer to frequency convert an output signal of said second LNA," and (c) the "second microelectronic chip" as further including "a voltage controlled oscillator to generate local oscillator signals for said first and second mixers, said third interconnect to carry a corresponding local oscillator signal to said first microelectronic die for use by said first mixer." Sugar et al. does not disclose such an arrangement.

Claim 12 adds: (a) a fourth microelectronic die that includes a third receiver front end and (b) a fourth interconnect between the fourth microelectronic die and the third microelectronic die, to the module of claim 1. Sugar et al. does not disclose such an arrangement. Claim 18 adds a "third LNA having a single-ended input to receive a signal from a third antenna" and "a third mixer to perform a frequency conversion on an amplified output signal of said third LNA" to claim 13. Sugar et al. does not disclose a receiver system that includes one LNA having a differential input to receive a signal from a first antenna and multiple other LNAs having single ended inputs to receive signals from other antennas.

Conclusion

Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (480-948-3745) to facilitate prosecution of this application.

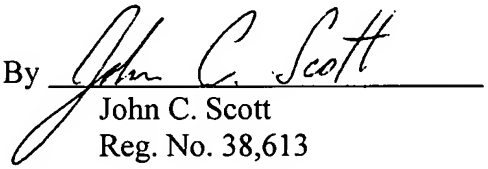
Respectfully submitted,

RONALD D. JAVOR, ET AL.

By their Representatives,

Customer Number: 45643
480-948-3745

Date February 20, 2007

By 
John C. Scott
Reg. No. 38,613

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Shellie Bailey